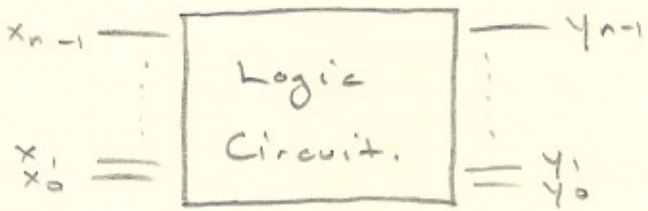
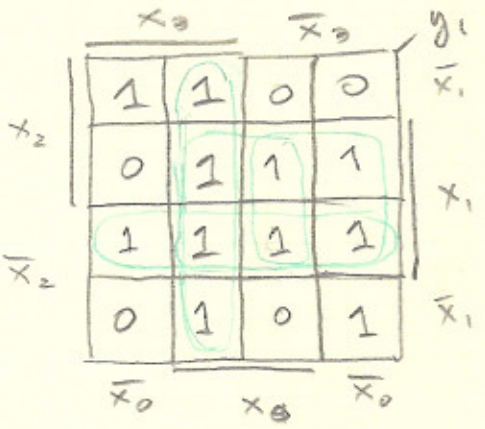
LOGIC CIRCUITS

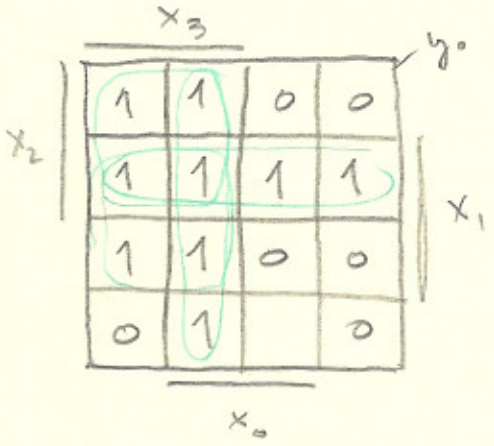


* Truth table
* Minimisation by Karnal map.
* Block diagram of circuit
* Design of CMOS circuit
* Simulation.

EX:

x_3	x_2	x_1	x_0	y_1	y_0
0	0	0	0	1	0
0	0	0	1	0	0
0	0	1	0	1	0
0	0	1	1	1	0
0	1	0	0	0	0
0	1	0	1	0	0
0	1	1	0	1	1
0	1	1	1	1	1
1	0	0	0	0	1
1	0	0	1	1	1
1	0	1	0	1	1
1	0	1	1	1	0
1	1	0	0	1	1
1	1	0	1	1	1
1	1	1	0	0	1
1	1	1	1	1	1

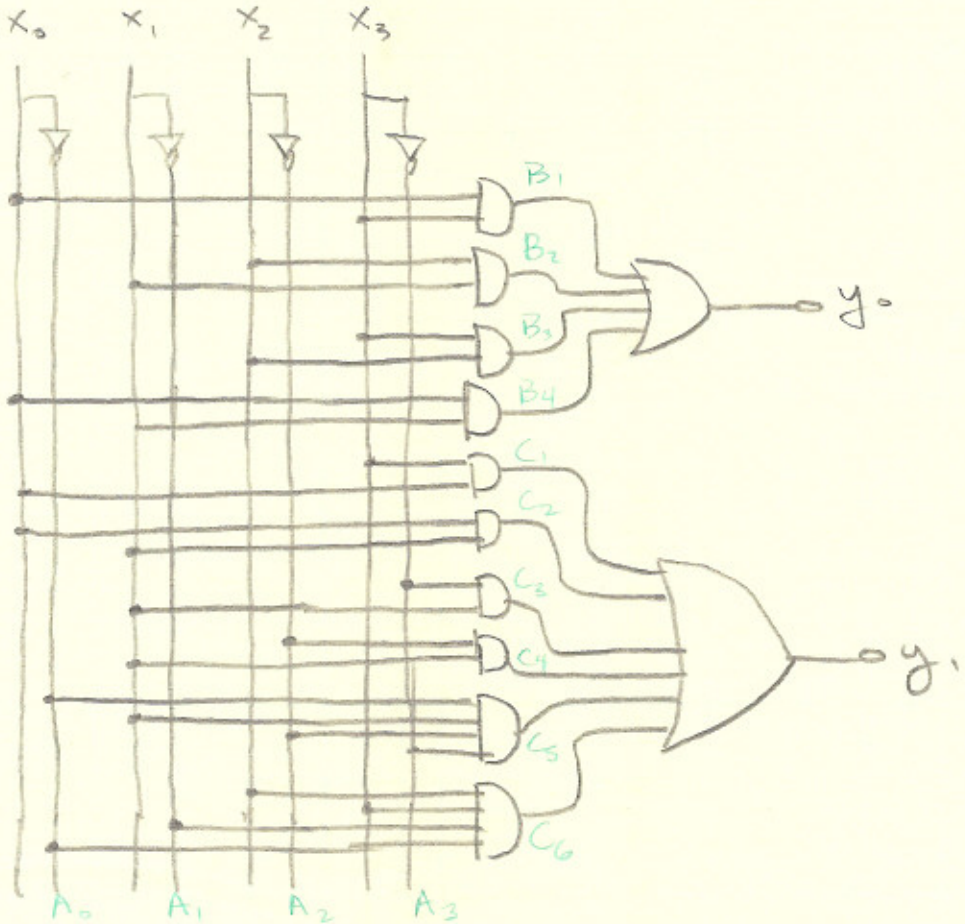




$$y_0 = x_3 \cdot x_0 + x_2 \cdot x_1 + x_3 \cdot x_2 + x_3 \cdot x_1$$

$$y_1 = x_3 \cdot x_0 + x_1 \cdot x_0 + \bar{x}_3 \cdot x_1 + \bar{x}_2 \cdot x_1$$

$$+ \bar{x}_0 \cdot x_1 \cdot \bar{x}_2 \cdot \bar{x}_3 + x_2 \cdot \bar{x}_1 \cdot \bar{x}_0 \cdot x_3$$



For the Design of complex Cmos; refer to CCD notes. Will need to know this for test.

For the Verilog simulation, all nodes must be labeled.

```
module circuit;
input x3, x2, x1, x0;
output y1, y0;
wire x3, x2, x1, x0, y1, y0, A0, A1, A2, B1, B2,
     B3, B4, C1, C2, C3, C4, C5, C6;

begin
fork
A3 = ! x3;
A2 = ! x2;
A1 = ! x1;
A0 = ! x0;

join

#2;

fork

B1 = x3 && x0;
B2 = x2 && x1;
B3 = x3 && x2;
B4 = x3 && x1;

C1 = x3 && x0;
C2 = x1 && x0;
C3 = A3 && x1;
C4 = A2 && x1;
C5 = A0 && x1 && A2 && A3;
C6 = x2 && A1 && A0 && x3;

join

#5;
fork

y0 = B1 || B2 || B3 || B4;
y1 = C1 || C2 || C3 || C4 || C5 || C6;
```

```
join
#4;
end
end module.
```

note

C = !A && B

we can't do this because there is more than one gate envolved.